Atty. Docket No. OF03P212/US
Serial No: 10/733,884

Remarks

The present invention relates to a semiconductor device and a method of manufacturing a semiconductor device having a plurality of via holes in each of a plurality of parts of an insulating layer. Each of the plurality of via holes in a given insulating layer part exposes a conductive line. In some aspects, each of the parts of the insulating layer (other than the via holes) has a certain thickness greater than zero but less than the insulating layer thickness (e.g., Claims 1 and 16), or a trenches are etched in the insulating layer such that each trench enables electrical connection of a subsequently formed conductive layer through a corresponding plurality of via holes to the exposed conductive line (e.g., Claim 10).

The reference cited against the originally-filed claims (Jahnes et al, U.S. Pat. No. 6,380,003 [hereinafter "Jahnes"]) neither discloses nor suggests forming a plurality of via holes in a part of an insulating layer having a thickness greater than zero but less than the insulating layer thickness (e.g., Claim 1), or etching trenches in the insulating layer having a width greater than a combined width of the plurality of via holes (e.g., Claim 10). Consequently, Jahnes neither discloses nor suggests a semiconductor device that contains a plurality of via holes in a part of an insulating layer having a thickness greater than zero but less than the insulating layer thickness (e.g., Claim 16), and the present claims are patentable over the cited reference.

The Rejection of Claims 1-5 under 35 U.S.C. § 102

The rejection of Claims 1-5 under 35 U.S.C. § 102(b) as being anticipated by Jahnes is respectfully traversed.

Jahnes discloses a substrate having a first level of electrically conductive features formed thereon; a patterned interlevel dielectric material formed on the substrate, wherein the patterned interlevel dielectric includes via spaces, and at least one of said via spaces is a slot via in which an anti-fuse material is formed on a portion thereof; and a second level of electrically conductive features formed in the spaces, whereby the anti-fuse material in the slot via provides a connection between the first and second levels of electrically conductive features (Abstract).

FIG. 2c discloses via 58 and slot via 60 formed in interlevel dielectric 54, to expose portions of the first level of electrically conductive features 52 (col. 4, ll. 21-29). Jahnes then teaches patterning a photoresist 64 to provide spaces 66 which correspond to positions in which the second level of electrically conductive features will subsequently be formed (col. 5, ll. 4-11; also see FIG. 2e). A portion of the patterned photoresist remains over the first level of electrically conductive features in the slot via (col. 5, ll. 11-14 and FIG. 2f).

However, Jahnes is silent with regard to forming a plurality of via holes in a part of an insulating layer having a thickness greater than zero but less than the insulating layer thickness (Claim 1). The only structure in which Jahnes appears to form a plurality of via "holes" is the insulator layer 54 itself. Thus, Jahnes does not disclose or suggest the method of the present Claim 1.

Claims 3-5 depend from Claim 1, and thus include all of the limitations of Claim 1. Therefore, Claims 3-5 are patentable over Jahnes for essentially the same reasons as Claim 1. Claim 2 has been cancelled. Consequently, this ground of rejection is unsustainable, and should be withdrawn.

Claims 16-21 Are Patentable over Jahnes

As explained above, the semiconductor device of the present Claim 16 has a plurality of via holes in each of a plurality of parts of an insulating layer, each such insulating layer part (other than the via holes) having a thickness greater than zero but less than the insulating layer thickness. As explained in part above, Jahnes discloses only a device having a single via hole 58 or via slot 60 in each any part of an insulating layer having a thickness greater than zero but less than the insulating layer thickness (such as spaces 66). The only structure in which Jahnes appears to form a plurality of via "holes" is the insulator layer 54 itself, rather than a part thereof having a thickness less than the insulating layer thickness.

Consequently, Jahnes does not disclose or suggest the device of new Claim 16. Claims 17-21 depend from Claim 16, and thus include all of the limitations of Claim 16. Therefore, Claims 17-21 are also patentable over Jahnes for essentially the same reasons as Claim 16.

Claims 10-15 Are Patentable over Jahnes

As explained above, the method of the present Claim 10 etches trenches that enable electrical connection of a subsequently formed conductive layer through a corresponding plurality of via holes to an exposed conductive line. As explained in part above, assuming for the sake of argument that the spaces 66 disclosed by Jahnes correspond to the trenches recited in the present Claim 10, each space 66 contains only a single via hole 58 or a small part of via slot 60 (see FIGS. 2f, 2g and 3). Thus, Jahnes does not appear to disclose or suggest forming a trench enabling electrical connection of a subsequently formed conductive layer through a plurality of via holes to an exposed conductive line. In fact, as explained above, one of the two vias disclosed by Jahnes, via slot 60, does not expose underlying conductive line 52 at all (see, e.g., col. 5, ll. 11-14 and FIG. 2f).

Consequently, Jahnes does not disclose or suggest the method of new Claim 10. Claims 11-15 depend from Claim 10, and thus include all of the limitations of Claim 10. Therefore, Claims 11-15 are also patentable over Jahnes for essentially the same reasons as Claim 10.

Conclusion

In view of the above amendments and remarks, the rejection is believed to be overcome, and the application is believed to be in condition for allowance. Early notice to that effect is earnestly requested.

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If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

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